CLAIMS

What is claimed is:

1. An on-chip loop filter for a phase locked loop, the on-chip filter comprises:

a first resistor having a first node and a second node, wherein the first node is operably coupled to receive a charge pump output;

a first capacitor having a first node and a second node, wherein the first node of the first capacitor is operably coupled in series with the second node of the first resistor, wherein the second node of the first capacitor is coupled to a return, wherein the first capacitor is of a first capacitor construct having a first quality factor;

a second capacitor operably coupled in parallel to the series connection of the first resistor and the first capacitor, wherein the second capacitor is of a second capacitor construct having a second quality factor, wherein the second quality factor is greater than the first quality factor;

a third capacitor operably coupled in parallel with the second capacitor, wherein the third capacitor is of third capacitor construct having a third quality factor, wherein the third quality factor is greater than the second quality factor;

a second resistor having a first node and a second node, wherein the first node of the second resistor is operably coupled to the first node of the first resistor; and

a fourth capacitor having a first node and a second node, wherein the first node of the fourth capacitor is coupled to the second node of the second resistor to provide a control voltage, wherein the second node of the fourth capacitor is coupled to the return, wherein the fourth capacitor is of the third capacitor construct having the third quality factor.

2. The on-chip loop filter of claim 1 further comprises:

the first capacitor having a first die area to capacitance ratio;

the second capacitor having a second die area to capacitance ratio; and

the third capacitor and fourth capacitors have a third die area to capacitance ratio, wherein the third die area to capacitance ratio is greater than the second die area to capacitance ratio, which is greater than the first die area to capacitance ratio.

3. The on-chip loop filter of claim 1 further comprises at least one of:

the first resistor including a variable resistance structure; and

the second resistor including a second variable resistance structure.

4. The on-chip loop filter of claim 1 further comprises at least one of:

the first capacitor including a variable capacitive structure;

the second capacitor including a second variable capacitive structure;

the third capacitor including a third variable capacitive structure; and

the fourth capacitor including a fourth variable capacitive structure.

5. The on-chip loop filter of claim 1, wherein the third capacitor construct comprises a metal fringe capacitor structure.

6. The on-chip loop filter of claim 1, wherein the second capacitor construct comprises a plurality of MOS (Metal Oxide Semiconductor) transistors, wherein each of the plurality of MOS transistors has a narrow channel length.

7. The on-chip loop filter of claim 1, wherein the third capacitor construct comprises a plurality of MOS (Metal Oxide Semiconductor) transistors, wherein each of the plurality of transistors has a wide channel length.

8. The on-chip loop filter of claim 1 further comprises:

the second capacitor fabricated on a first metal layer; and

the third capacitor fabricated on a second metal layer, wherein the second capacitors substantially overlays the third capacitor.

9. The on-chip loop filter of claim 1 further comprises:

a ground plane fabricated to shield the first resistor, the first capacitor, the second capacitor, and the third capacitor.

10. The on-chip loop filter of claim 1 further comprises:

the second resistor and the fourth capacitor fabricated proximal to an input of a voltage controlled oscillator.

11. An on-chip phase locked loop comprises:

an oscillation comparator operably coupled to compare a reference oscillation with a feedback oscillation to determine at least one of a phase difference and a frequency difference;

a charge pump operably coupled to convert the at least one of the phase difference and the frequency difference into a charge pump signal;

a loop filter operably coupled to convert the charge pump signal into a control voltage;

a voltage controlled oscillator operably coupled to convert the control voltage into an output oscillation; and

a feedback module operably coupled to produce the feedback oscillation from the output oscillation, wherein the loop filter includes:

a first resistor having a first node and a second node, wherein the first node is operably coupled to receive the charge pump signal;

a first capacitor having a first node and a second node, wherein the first node of the first capacitor is operably coupled in series with the second node of the first resistor, wherein the second node of the first capacitor is coupled to a return, wherein the first capacitor is of a first capacitor construct having a first quality factor;

a second capacitor operably coupled in parallel to the series connection of the first resistor and the first capacitor, wherein the second capacitor is of a second capacitor construct having a second quality factor, wherein the second quality factor is greater than the first quality factor;

a third capacitor operably coupled in parallel with the second capacitor, wherein the third capacitor is of third capacitor construct having a third quality factor, wherein the third quality factor is greater than the second quality factor;

a second resistor having a first node and a second node, wherein the first node of the second resistor is operably coupled to the first node of the first resistor; and

a fourth capacitor having a first node and a second node, wherein the first node of the fourth capacitor is coupled to the second node of the second resistor to provide the control voltage, wherein the second node of the fourth capacitor is coupled to the return, wherein the fourth capacitor is of the third capacitor construct having the third quality factor.

12. The on-chip phase locked loop of claim 11 further comprises:

the first capacitor having a first die area to capacitance ratio;

the second capacitor having a second die area to capacitance ratio; and

the third capacitor and fourth capacitors have a third die area to capacitance ratio, wherein the third die area to capacitance ratio is greater than the second die area to capacitance ratio, which is greater than the first die area to capacitance ratio.

13. The on-chip phase locked loop of claim 11 further comprises at least one of:

the first resistor including a variable resistance structure; and

the second resistor including a second variable resistance structure.

14. The on-chip phase locked loop of claim 11 further comprises at least one of:

the first capacitor including a variable capacitive structure;

the second capacitor including a second variable capacitive structure;

the third capacitor including a third variable capacitive structure; and

the fourth capacitor including a fourth variable capacitive structure.

15. The on-chip phase locked loop of claim 11, wherein the third capacitor construct comprises a metal fringe capacitor structure.

16. The on-chip phase locked loop of claim 11, wherein the second capacitor construct comprises a plurality of MOS (Metal Oxide Semiconductor) transistors, wherein each of the plurality of MOS transistors has a narrow channel length.

17. The on-chip phased locked loop of claim 11, wherein the third capacitor construct comprises a plurality of MOS (Metal Oxide Semiconductor) transistors, wherein each of the plurality of transistors has a wide channel length.

18. The on-chip phased locked loop of claim 11 further comprises:

the second capacitor fabricated on a first metal layer; and

the third capacitor fabricated on a second metal layer, wherein the second capacitors substantially overlays the third capacitor.

19. The on-chip phased locked loop of claim 11 further comprises:

a ground plane fabricated to shield the first resistor, the first capacitor, the second capacitor, and the third capacitor.

20. The on-chip phased locked loop of claim 11 further comprises:

the second resistor and the fourth capacitor fabricated proximal to an input of a voltage controlled oscillator.

21. A radio frequency integrated circuit (RFIC) comprises:

a receiver section operably coupled to convert inbound radio frequency (RF) signals into inbound baseband signals in accordance with a receiver local oscillation;

a transmitter section operably coupled to convert outbound baseband signals into output RF signals in accordance with a transmitter local oscillation; and

a local oscillation module operably coupled to produce the receiver local oscillation and the transmitter local oscillation, wherein the local oscillation module includes:

an oscillation comparator operably coupled to compare a reference oscillation with a feedback oscillation to determine at least one of a phase difference and a frequency difference;

a charge pump operably coupled to convert the at least one of the phase difference and the frequency difference into a charge pump signal;

a loop filter operably coupled to convert the charge pump signal into a control voltage;

a voltage controlled oscillator operably coupled to convert the control voltage into an output oscillation, wherein the receiver local oscillation and the transmitter local oscillation are derived from the output oscillation; and

a feedback module operably coupled to produce the feedback oscillation from the output oscillation, wherein the loop filter includes:

a first resistor having a first node and a second node, wherein the first node is operably coupled to receive the charge pump signal;

a first capacitor having a first node and a second node, wherein the first node of the first capacitor is operably coupled in series with the second node of the first resistor, wherein the second node of the first capacitor is coupled to a return, wherein the first capacitor is of a first capacitor construct having a first quality factor;

a second capacitor operably coupled in parallel to the series connection of the first resistor and the first capacitor, wherein the second capacitor is of a second capacitor construct having a second quality factor, wherein the second quality factor is greater than the first quality factor;

a third capacitor operably coupled in parallel with the second capacitor, wherein the third capacitor is of third capacitor construct having a third quality factor, wherein the third quality factor is greater than the second quality factor;

a second resistor having a first node and a second node, wherein the first node of the second resistor is operably coupled to the first node of the first resistor; and

a fourth capacitor having a first node and a second node, wherein the first node of the fourth capacitor is coupled to the second node of the second resistor to provide the control voltage, wherein the second node of the fourth capacitor is coupled to the return, wherein the fourth capacitor is of the third capacitor construct having the third quality factor.

22. The RFIC of claim 21 further comprises:

the first capacitor having a first die area to capacitance ratio;

the second capacitor having a second die area to capacitance ratio; and

the third capacitor and fourth capacitors have a third die area to capacitance ratio, wherein the third die area to capacitance ratio is greater than the second die area to capacitance ratio, which is greater than the first die area to capacitance ratio.

23. The RFIC of claim 21 further comprises at least one of:

the first resistor including a variable resistance structure; and

the second resistor including a second variable resistance structure.

24. The RFIC of claim 21 further comprises at least one of:

the first capacitor including a variable capacitive structure;

the second capacitor including a second variable capacitive structure;

the third capacitor including a third variable capacitive structure; and

the fourth capacitor including a fourth variable capacitive structure.

25. The RFIC of claim 21, wherein the third capacitor construct comprises a metal fringe capacitor structure.

26. The RFIC of claim 21, wherein the second capacitor construct comprises a plurality of MOS (Metal Oxide Semiconductor) transistors, wherein each of the plurality of MOS transistors has a narrow channel length.

27. The RFIC of claim 21, wherein the third capacitor construct comprises a plurality of MOS (Metal Oxide Semiconductor) transistors, wherein each of the plurality of transistors has a wide channel length.

28. The RFIC of claim 21 further comprises:

the second capacitor fabricated on a first metal layer; and

the third capacitor fabricated on a second metal layer, wherein the second capacitors substantially overlays the third capacitor.

29. The RFIC of claim 21 further comprises:

a ground plane fabricated to shield the first resistor, the first capacitor, the second capacitor, and the third capacitor.

30. The RFIC of claim 21 further comprises:

the second resistor and the fourth capacitor fabricated proximal to an input of a voltage controlled oscillator.